Please amend claims 1, 4, 9, 12, 17 and 19, as provided in the APPENDIX A attached hereafter and showing the clean version of the entire set of pending claims. The "marked-up" version of the amended claims are provided in the APPENDIX B attached hereafter.

REMARKS

In response to the Office Action dated August 28, 2002, claims 8 and 16 have been cancelled, claims 1, 4, 9, 12, 17 and 19 have been amended, and claims 21-23 are newly added. Claims 1-7, 9-15 and 17-23 are now active in this application, of which claims 1, 4, 12, 17, 19 and 21 are independent. The Office Action indicates that claims 8-15 and 17-20 are objected to but allowable if presented in independent form.

Based on the above Amendments and the following Remarks, Applicants respectfully request that the Examiner reconsider the outstanding objections and rejections and they be withdrawn.

Rejections Under 35 U.S.C. §103

In the Office Action, claims 1-6 and 16 have been rejected under 35 U.S.C. §103(a) for being unpatentable over U. S. Patent No. 6,229,516 issued to Kim, *et al.* ("Kim") in view of Japanese Patent Publication No. 03-125187 issued to Konoue, *et al.* ("Konoue"). This rejection is respectfully traversed.

In this response, independent claim 16 has been cancelled and its allowable dependent claims 17 and 19 have been amended to present in independent from by incorporating all of the limitations of claim 16.

Also, independent claims 1 and 4 have been amended to include the subject matter recited in allowable claim 8. More specifically, amended independent claim 1 recites "wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction from a first gate line to a last gate line of said second gate line block.

Similarly, amended independent claim 4 recites "wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in a direction from a last gate line to a first gate line thereof, and the second gate driver sequentially supplies the scanning signals to the second gate lines in a direction from a first gate line to a last gate line thereof".

Thus, it is submitted that independent claims 1 and 4 are patentable over Kim and Konoue. Claims 2, 3, 5 and 6 that are dependent from claims 1 and 4 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request that the rejection over claims 1-6 and 16 be withdrawn.

In the Office Action, claim 7 has been rejected under 35 U.S.C. §103(a) over Kim in view of Konoue and further in view of Tanioka, et al. (U. S. Patent No. 5,093,655). This rejection is respectfully treversed.

Claim 7 is dependent from independent claim 4. As previously mentioned, claim 4 has been amended and is now believed to be patentable over Kim and Konoue. Particularly, claim 4 recites "wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in a direction from a last gate line to a first gate line thereof, and the second gate driver

sequentially supplies the scanning signals to the second gate lines in a direction from a first gate line to a last gate line thereof".

In this regard, Tanioka is directed to reversing polarity of the picture signals in adjacent columns in order to visually compensate the flickers of the entire face of an LCD, but Tanioka fails to teach or suggest the newly added limitations of claim 4. Thus, Tanioka fails to cure the deficiency from teachings of Kim and Konoue.

It is respectfully submitted that claim 4 is patentable over Kim, Konoue and Tanioka. Thus, claim 7 that is dependent from claim 4 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request that the rejection over claim 7 be withdrawn.

Other Matters

In this response, allowable dependent claim 12 has been amended to present in independent from by incorporating all of the limitations of independent claim 4. Also, allowable dependent claims 17 and 19 have been amended to present in independent form by incorporating all of the limitations of independent claim 16. Also, since claim 8 has been incorporated into independent claim 4, claim 9 has been amended to be dependent from claim 4.

Further, claims 21-23 are newly added. Independent claim 21 claims the subject matter of originally filed claims 1 and 12.

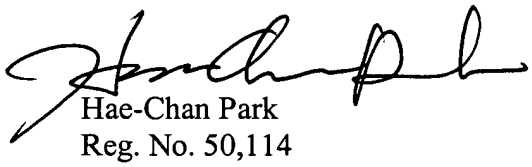
CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner

reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 1-7, 9-15 and 17-23 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,



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APPENDIX A

The clean version of the entire set of pending claims is as follows. The "marked-up" version of the amended claims is provided in the APPENDIX B hereafter.

Sub C1

1. (Amended) A liquid crystal display (LCD), comprising:

a first gate line block including a plurality of first gate lines transmitting scanning signals;

a second gate line block including a plurality of second gate lines transmitting scanning signals, scanning directions of the first gate lines being opposite to scanning directions of the second gate lines;

B1

a plurality of first data lines transmitting image signals and crossing the first gate lines of the first gate line block;

a plurality of second data lines separated from the first data lines and crossing the second gate lines of the second gate line block;

a plurality of pixels configured in a matrix pattern and defined by the gate lines and data lines, and including switching elements coupled to the gate lines and the data lines,

wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction from a first gate line to a last gate line of said second gate line block.

Sub C1

2. The LCD of claim 1, wherein a number of the first gate lines is equal to a number of the second gate lines.

3. The LCD of claim 2, wherein the first gate lines and the second gate lines are simultaneously scanned.

4. (Twice Amended) A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line block having a plurality of second gate lines, said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

a plurality of second data lines crossing and separated from the second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals, to the first data lines;

a second data driver supplying data voltages, which contain image signals, to the second data lines;

a first gate driver supplying scanning signals to the gate lines of said first gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

a first frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals,

wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in a direction from a last gate line to a first gate line thereof, and the second gate driver sequentially supplies the scanning signals to the second gate lines in a direction from a first gate line to a last gate line thereof.

5. The LCD of claim 4, wherein a number of the first gate lines is equal to a number of the second gate lines.

6. The LCD of claim 5, wherein the first gate driver and the second gate driver are simultaneously scanned.

7. The LCD of claim 5, wherein polarities of the data voltages supplied to the pixels coupled to adjacent gate lines of the first gate line block are opposite to each other with respect to the common voltage, and the polarities of the data voltages supplied to the pixels coupled to the neighboring gate lines of the second gate line block are opposite to each other with respect to the common voltage.

8. Cancelled.

Sub C1 B3

9. (Amended) The LCD of claim [8] 4, wherein the first frame memory outputs the image signals, which are written in opposite order from the image signals to be provided to the first data lines, to the first data driver, and the second frame memory outputs the image signals, which are written in identical order from the image signals to be provided to the second data lines, to the second data driver.

Sub C1

10. The LCD of claim 9, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of the first gate line block, is opposite to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of the second gate line block on the identical pixel row.

11. The LCD of claim 9, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of the first gate line block, is identical with that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of the second gate line block on the identical pixel row.

Sub B4 C1

12. (Amended) A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line block having a plurality of second gate lines, said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

a plurality of second data lines crossing and separated from the second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals, to the first data lines;

B4 Cont

a second data driver supplying data voltages, which contain image signals, to the second data lines;

a first gate driver supplying scanning signals to the gate lines of said first gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

a first frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals;

wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in a direction from a first gate line to a last gate line thereof, and the second gate driver

B4 cont.

sequentially supplies the scanning signals to the second gate lines in a direction from a last gate line to a first gate line thereof.

Sub C1

13. The LCD of claim 12, wherein the first frame memory outputs the image signals, which are written in an identical order as the image signals to be provided to the first data lines, to the first data driver, and the second frame memory outputs the image signals, which are written in an opposite order as the image signals to be provided to the second data lines, to the second data driver.

14. The LCD of claim 13, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of the first gate line block, is opposite to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of the second gate line block on the identical pixel row.

15. The LCD of claim 13, wherein the polarity of the common voltage with respect to the data voltage supplied to the pixels coupled to the last gate line of the first gate line block, is identical with that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of the second gate line block on the identical pixel row.

16. Cancelled.

B5 Sub C1

17. (Amended) A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the

first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

providing sequentially scanning signals to the first gate lines of the first gate line block;

providing sequentially scanning signals to the second gate lines of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided,

wherein the scanning signals are sequentially provided to the first gate line block in a direction from a last gate line to a first gate line thereof, and to the second gate line block in a direction from a first gate line to a last gate line thereof.

18. The method of claim 17, wherein the method further comprises the steps of:

writing the image signals to be provided to the first data line to the first frame memory, the image signals received externally;

writing the image signals to be provided to the second data line to the second frame memory, the image signals received externally;

outputting the image signals to the first data lines in an opposite order as the image signals to be written to the first frame memory; and

outputting the image signals to the second data lines in an opposite order as the image signals to be written to the second frame memory.

Sub C1

19. (Amended) A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

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providing sequentially scanning signals to the first gate lines of the first gate line block;

providing sequentially scanning signals to the second gate lines of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided,

wherein the scanning signals are sequentially provided to the first gate line block in a direction from a first gate line to a last gate line thereof, and to the second gate line block in a direction from a last gate line to a first gate line thereof.

Sub C1

20. The method of claim 19, wherein the method further comprises the steps of:

writing the image signals to be provided to the first data line to the first frame memory, the image signals received externally;

writing the image signals to be provided to the second data line to the second frame memory, the image signals received externally;

outputting the image signals to the first data lines in an opposite order as the image signals to be written to the first frame memory; and

outputting the image signals to the second data lines in an opposite order as the image signals to be written to the second frame memory.

Sub C1

21. (Newly Added) A liquid crystal display (LCD), comprising:

a first gate line block including a plurality of first gate lines transmitting scanning signals;

a second gate line block including a plurality of second gate lines transmitting scanning signals, scanning directions of the first gate lines being opposite to scanning directions of the second gate lines;

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a plurality of first data lines transmitting image signals and crossing the first gate lines of the first gate line block;

a plurality of second data lines separated from the first data lines and crossing the second gate lines of the second gate line block;

a plurality of pixels configured in a matrix pattern and defined by the gate lines and data lines, and including switching elements coupled to the gate lines and the data lines,

wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, the scanning signals are sequentially supplied to said second gate line block in a direction from a last gate line to a first gate line thereof.

22. (Newly Added) The LCD of claim 21, wherein a number of the first gate lines is equal to a number of the second gate lines.

B7 cont.

23. (Newly Added) The LCD of claim 22, wherein the first gate lines and the second gate lines are simultaneously scanned.

APPENDIX B

The "marked-up" version of the amended claims is as follows:

1. (Amended) A liquid crystal display (LCD), comprising:

a first gate line block including a plurality of first gate lines transmitting scanning signals;

a second gate line block including a plurality of second gate lines transmitting scanning signals, scanning directions of the first gate lines being opposite to scanning directions of the second gate lines;

a plurality of first data lines transmitting image signals and crossing the first gate lines of the first gate line block;

a plurality of second data lines separated from the first data lines and crossing the second gate lines of the second gate line block;

a plurality of pixels configured in a matrix pattern and defined by the gate lines and data lines, and including switching elements coupled to the gate lines and the data lines,

wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a last gate line to a first gate line thereof, and the scanning signals are sequentially supplied to said second gate line block in a direction from a first gate line to a last gate line of said second gate line block.

4. (Twice Amended) A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line block having a plurality of second gate lines, said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

a plurality of second data lines crossing and separated from the second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals, to the first data lines;

a second data driver supplying data voltages, which contain image signals, to the second data lines;

a first gate driver supplying scanning signals to the gate lines of said first gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

a first frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals.

wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in a direction from a last gate line to a first gate line thereof, and the second gate driver sequentially supplies the scanning signals to the second gate lines in a direction from a first gate line to a last gate line thereof.

9. (Amended) The LCD of claim [8] 4, wherein the first frame memory outputs the image signals, which are written in opposite order from the image signals to be provided to the first data lines, to the first data driver, and the second frame memory outputs the image signals, which are written in identical order from the image signals to be provided to the second data lines, to the second data driver.

12. (Amended) [The LCD of claim 7,] A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line block having a plurality of second gate lines, said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

a plurality of second data lines crossing and separated from the second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals, to the first data lines;

a second data driver supplying data voltages, which contain image signals, to the second data lines;

a first gate driver supplying scanning signals to the gate lines of said first gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

a first frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals,

wherein the first gate driver sequentially supplies the scanning signals to the first gate lines in [the] a direction from [the] a first gate line [of the first gate line block] to [the] a last gate line thereof, and the second gate driver sequentially supplies the scanning signals to the second gate lines in [the] a direction from [the] a last gate line [of the second gate line block] to [the] a first gate line thereof.

17. (Amended) [The method of claim 16,] A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line

block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

providing sequentially scanning signals to the first gate lines of the first gate line block;

providing sequentially scanning signals to the second gate lines of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided,

wherein the scanning signals are sequentially provided to the first gate line block in [the] a direction from [the] a last gate line to [the] a first gate line thereof, and to the second gate line block in [the] a direction from [the] a first gate line to [the] a last gate line thereof.

19. (Amended) [The method of claim 16,] A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

providing sequentially scanning signals to the first gate lines of the first gate line block;

providing sequentially scanning signals to the second gate lines of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided,

wherein the scanning signals are sequentially provided to the first gate line block in [the] a direction from [the] a first gate line to [the] a last gate line thereof, and to the second gate line block in [the] a direction from [the] a last gate line to [the] a first gate line thereof.

Please add new claims 21-23, as follows.

21. (Newly Added) A liquid crystal display (LCD), comprising:

a first gate line block including a plurality of first gate lines transmitting scanning signals;

a second gate line block including a plurality of second gate lines transmitting scanning signals, scanning directions of the first gate lines being opposite to scanning directions of the second gate lines;

a plurality of first data lines transmitting image signals and crossing the first gate lines of the first gate line block;

a plurality of second data lines separated from the first data lines and crossing the second gate lines of the second gate line block;

a plurality of pixels configured in a matrix pattern and defined by the gate lines and data lines, and including switching elements coupled to the gate lines and the data lines,

wherein the scanning signals are sequentially supplied to said first gate line block in a direction from a first gate line to a last gate line thereof, the scanning signals are sequentially

supplied to said second gate line block in a direction from a last gate line to a first gate line thereof.

22. (Newly Added) The LCD of claim 21, wherein a number of the first gate lines is equal to a number of the second gate lines.

23. (Newly Added) The LCD of claim 22, wherein the first gate lines and the second gate lines are simultaneously scanned.